From StrongArm™ to PWRficient™: The Battle to Reduce Power in Microprocessors

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The Escalating Power Problem

- Shrinking device geometries provides:
  - Faster gates
  - Increased density

BUT

- Moore’s Law means more power

EXCESSIVE POWER DISSIPATION LIMITS USABLE GATE CAPACITY
Operating Costs of High-End Servers

- Total cost = acquisition cost + operating cost*

- Over a five-year period, operating costs exceed acquisition costs
  - Operating costs dominated by the cost of power and air-conditioning

POWER-EFFICIENT PROCESSORS CAN LEAD TO SIGNIFICANT OPERATING-COST SAVINGS FOR DATA CENTERS

*See P.A. Semi white paper PWRficient-Based Supercomputing
Power Constraints for Consumer Applications

- Multiple functions are converging in consumer appliances
  - e.g., home gateway/media center/NAS
  - Increased performance demands

- Consumer applications favor fanless, low-power operation
  - Conventional TDP-limited solutions compromise performance

CONSUMER APPLICATIONS REQUIRE INCREASING PROCESSOR PERFORMANCE WITHIN SEVERE POWER LIMITS
System Power

- Power is a system problem
  - Power reduction needs to go beyond CPU

- Major components of system power other than the processor
  - Memory power
  - Power in other external components
  - Chip-to-chip interconnect power
  - Power supply losses

ALL MAJOR COMPONENTS OF SYSTEM POWER MUST BE REDUCED FOR BEST OVERALL POWER EFFICIENCY
Understanding Power Basics
CMOS Power Basics

Switching Power
\[ P = N_{\text{switch}} \times F \times C \times V_{dd}^2 \]

Short Circuit Power
\[ P = N_{\text{switch}} \times F \times V_{dd} \times I_{sc} \]

Leakage Power
\[ P = N \times I_{\text{leak}} \times V_{dd} \]

\[ I_{sc} \propto V_{dd}, I_{\text{leak}} \propto V_{dd}, N_{\text{switch}} = \psi \times N \]

\[ P = V_{dd}^2 \times N \times [\psi \times F \times (C + \varepsilon_{sc}) + \gamma_{\text{leak}}] \]

- \( V_{dd} \): PS voltage
- \( N \): Total number of gates
- \( \psi \): Fraction of gates switching per clock cycle
- \( F \): Clock frequency
- \( C \): Average capacitative loading of a single gate
- \( \varepsilon_{sc} \): Short circuit factor of average gate
- \( \gamma_{\text{leak}} \): Leakage factor of average gate
A Few More Basics

Gate Delay $\alpha \frac{\lambda}{(V_{dd} - V_t)}$

so

$F_{max} \propto \frac{(V_{dd} - V_t)}{\lambda}$

and

$\gamma_{leak} \propto e^{-V_t}$

$N \propto \frac{1}{\lambda^2}$

$C \propto \lambda$

$\varepsilon_{sc} \propto \lambda$

where

$\lambda$ Minimum feature size

$F_{max}$ Maximum clock frequency

$N$ Total number of gates

$C$ Average capacitative loading of a single gate

$V_t$ Transistor threshold voltage
From StrongARM to PWRficient
StrongARM Raised the Power-Efficiency Bar

- **Low-power design**
  - Built on the high-performance design methodology developed for Alpha™

- **50x performance/Watt improvement over Alpha**
  - Integer performance nearly equivalent to original 21064 Alpha
  - 0.5W power dissipation (StrongARM) compared with 26W (Alpha)
StrongARM Features

- **Functionality:**
  - 160MHz integer core
  - Including a 32b MAC unit
  - Simple 5 stage pipeline
  - 16KB L1 I + D Caches
  - External address and data bus
  - Idle and sleep modes

- **Technology:**
  - 0.35um CMOS
  - 1.65V $V_{dd}$
  - 0.35V $V_t$
  - 250K logic transistors

- **Power:**
  - 0.5W @ 160MHz

- **Performance:**
  - 185 Dhrystone MIPS
StrongARM’s improved power efficiency was achieved by the following first-order design and technology scaling

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ratio</th>
<th>Power Factor</th>
<th>Cumulative Improvement</th>
<th>Power 26W</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>3.45/1.5</td>
<td>5.3</td>
<td>5.3</td>
<td>4.9W</td>
</tr>
<tr>
<td>$N$</td>
<td>750K/250K</td>
<td>3</td>
<td>16.9</td>
<td>1.6W</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.75/0.35</td>
<td>2</td>
<td>33.8</td>
<td>0.8W</td>
</tr>
<tr>
<td>$\psi$</td>
<td>1.3</td>
<td>1.3</td>
<td>44</td>
<td>0.6W</td>
</tr>
<tr>
<td>$F$</td>
<td>200/160</td>
<td>1.25</td>
<td>55</td>
<td>0.5W</td>
</tr>
</tbody>
</table>
PWRficient PA6T Core

- **Functionality:**
  - 2.0GHz 64-bit core with FP and VMX
  - Super-scalar, out-of-order design
    - Quad-fetch, triple issue
  - 64KB L1 I + D Caches
  - Interface to on-chip coherent bus
  - Idle and sleep modes

- **Technology**
  - 65nm CMOS
  - 0.6–1.2V $V_{dd}$
  - 0.3V $V_t$
  - 11M logic transistors

- **Power**
  - 7W @ 2.0GHz

- **Performance**
  - SPECint®2000 >1000 per core
  - SPECfp®2000 >2000 per core
Exceptional performance-per-Watt

- PWRficient vs. dual 970 with discrete system controller, southbridge
  - Better integration
  - Lower latency
  - Application offloads
  - 5–10x power advantage

- PWRficient vs. Freescale 8641D
  - 64-bit vs. 32-bit
  - 2–4x performance advantage
  - 10GbE vs. GbE
  - More application offloads
  - > 3x power advantage

- PWRficient vs. Intel Yonah
  - Better integration
  - Lower latency
  - 3–5x power advantage
Comparing StrongARM and PWRficient

- Same basic design philosophy — balance power and performance

- Cores have a lot in common, despite their disparity in complexity
  - 250K vs. 11M transistors
  - Separated by 5 generations of technology
    \[ 2^5 \times 250K = 8M \]
  - Comparable footprint \(~10mm^2\) (not including L1 caches)
  - Excellent performance/Watt compared to competition
  - Very good absolute performance relative to much higher power competitors
From StrongARM to PWRficient

- Assume the PWRficient core is scaled from the StrongARM core
  - Using the same design techniques
  - Ignoring the significant increase in leakage current with technology scaling

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ratio</th>
<th>Power Factor</th>
<th>Cumulative Improvement</th>
<th>Power 0.5W</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>1.5/1.1</td>
<td>1.86</td>
<td>1.86</td>
<td>0.27W</td>
</tr>
<tr>
<td>$N$</td>
<td>250/11,000</td>
<td>0.023</td>
<td>0.042</td>
<td>11.83W</td>
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<tr>
<td>$\lambda$</td>
<td>0.35/0.065</td>
<td>5.4</td>
<td>0.23</td>
<td>2.2W</td>
</tr>
<tr>
<td>$\psi$</td>
<td>1.0</td>
<td>1.0</td>
<td>0.23</td>
<td>2.2W</td>
</tr>
<tr>
<td>$N$</td>
<td>160/2,000</td>
<td>0.08</td>
<td>0.0316</td>
<td>27.5W</td>
</tr>
</tbody>
</table>

- The analysis predicts that the new core should dissipate 27.5W
- Adding in the leakage factor adds another 5.5W, bringing the total expected power up to 33W!
The Factor of Four

How did PA Semi achieve a > 4× improvement in power efficiency over the StrongARM design?

We utilized two major techniques

- **Device-Specific $V_{dd}$ — 2× improvement factor**
  - Although the nominal $V_{dd}$ for the 65nm process is 1.1V, the design allows for a $V_{dd}$ that is specific to the device and conditions
  - To get the largest dynamic range possible, the caches are operated on a separate power supply

- **Ultra-fine-grained conditional clocking — 2× improvement factor**
  - The PA6T core takes clock gating to another level
  - Approximately 15K individually gated clocks for dual-core processor
Benefit of Device-Specific $V_{dd}$

- Fast parts tend to be very leaky

- Conventional approach
  - Operate at 1.1V across entire process range

- P.A. Semi approach
  - Operate at optimal device-specific $V_{dd}$
  - Partition power plane for optimal voltage selection per region

- Enables full process range for power yield
Ultra-Fine-Grained Clock Gating

% of Flops Clocked

Reset and flop initialization
Normal Operation
Thermal virus

Time
What Next?

► Pure scaling of the StrongARM design would have resulted in a power increase of > 50× due to basic physics

► P.A. Semi added two new techniques to those used in the original StrongARM and was able to improve on scaling by a factor of 4×, resulting in an increase of “only” 14× in power dissipation

CAN DESIGN ENGINEERS CONTINUE TO INNOVATE AT THE CIRCUIT LEVEL AND STEM THE SCALING TYRANNY OF NUMBERS?
Frequency is a dirty word with respect to power; recall

\[ P = V_{dd}^2 \times N \times [\psi \times F \times (C + \varepsilon_{sc}) + \gamma_{leak}] \]

and \( F_{\text{max}} \propto (V_{dd} - V_t) / \lambda \)

so if \( V_{dd} = f(F_{\text{max}}) \), then \( P_{F_{\text{max}}} \propto F_{\text{max}}^3 \)

Note that performance is \( \alpha F_{\text{max}} \), but

\[
\begin{array}{c|c|c}
\text{Performance} & \alpha & \frac{1}{F_{\text{max}}^2} \\
\hline
\text{Power} & & \\
\end{array}
\]
Parallel Processing

- Performance, Power and... Parallelism
- To a first order, if we take a computational task and
  - split it into two halves
  - operate each half at half the original frequency
  then we have improved the performance/power ratio by a factor of

\[ P_2 = \frac{F_{\text{max}}^3}{2 \times (F_{\text{max}}/2)^3} = 2^2 \]

- In general the parallelism improvement factor is

\[ P_N = N^2 \]

- This looks great, have we found the solution to our power problem?
The Problems with Parallelism

Three major limits to parallelism

- Decomposition is not always possible, especially at higher levels of N
- There is overhead required to recompose the solution
- There are limits to the amount of scaling that can be applied to $V_{dd}$ without hitting functionality limit

Still, parallelism is an important method

- Will continue to be a major theme of future chip developments
Memory

- **On-chip memories are power efficient**
  - RAM structures have low power density due to low inherent utilization
    - Only a few of many bit cells accessed per cycle
  - On-chip RAMs save power by avoiding chip-to-chip bus structures

- **Most on-chip memory is devoted to caches**
  - Caches have diminishing (logarithmic) performance return vs. size
Summarizing Trends

- Frequency scaling will slow down or stop
- Ultra-low voltage operation will be pursued
- Various types of parallelism will be exploited
  - Multi-core
  - Parallel vector engines, array processing in general
  - Whatever other parallelisms architects can think up and software can utilize
- More die area devoted to RAM-like structures
What’s Next for P.A. Semi

- Extend techniques further
  - Extend to even lower voltage operation
  - Add more power-saving modes

- Core evolution
  - Other performance/power points
  - Evolving with Power Architecture

- Parallelism roadmap
  - Quad core and beyond
    - VMX roadmap
    - Scaling L2 cache size, number
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